Programming the Artix-7 FPGA to Check its Basic Functions with the Development Test Board

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Since several detectors at Jefferson Lab use Xilinx Artix-7 field programmable gate arrays (FPGAs) in their front-end electronics, a test station is under development to perform basic functionality tests on an Artix-7 test board. First impression of the Artix-7 FPGA and preliminary results of the functionality tests are discussed.

Hall B RICH and Hall D DIRC use identical readout electronics for data acquisition. These detectors' front-end electronics tiles have the following components:

- a board with connectors that distribute high voltage to each multi-anode photomultiplier tubes (MAPMTs)
- for each MAPMT, a preamplifier-and-signal-shaper board, with multi-anode readout chips for each MAPMT channel
- an FPGA board with a Xilinx Artix7 that handles data transmission to the back-end electronics.

DSG procured a Diligent NEXYS4-DDR Artix-7 FPGA test board (Fig. 1) to perform basic FPGA functionality tests.

Programs were developed to test the basic functions of the FPGA and components on its development board. These programs verified that switches, various LED indicators, push buttons, and the FPGA's internal clock operated correctly. Additionally, programs were developed to convert binary number (input using development board's switches) to a decimal and display a looping count from 0—9 on the test board's LED digit indicators.

During development of the tests, a major obstacle faced was learning how to program the FPGA test board using Xilinx's Vivado IDE and compiler. Vivado uses Verilog, a hardware description language, to program the FPGA. While Verilog is similar to C, there are some differences between Verilog and C that added to the initial difficulty in developing test station programs to test the board's components.

Configuring the clock in the FPGA's program had issues. The clocking signal of the FPGA could not be changed from its default period of 20 ns. After investigation, a second clock had to be generated from the primary 20-ns clock to meet the clocking specifications in the test programs.

Initial impressions of the Xilinx Artix-7 FPGA development board are that it communicated to the components, and the components on the board work correctly. Future tests of the Artix-7 test board include testing its data communication capabilities, testing the maximum size of data that can be transferred without error at the maximum clock speed, and testing its capabilities in remote communication.

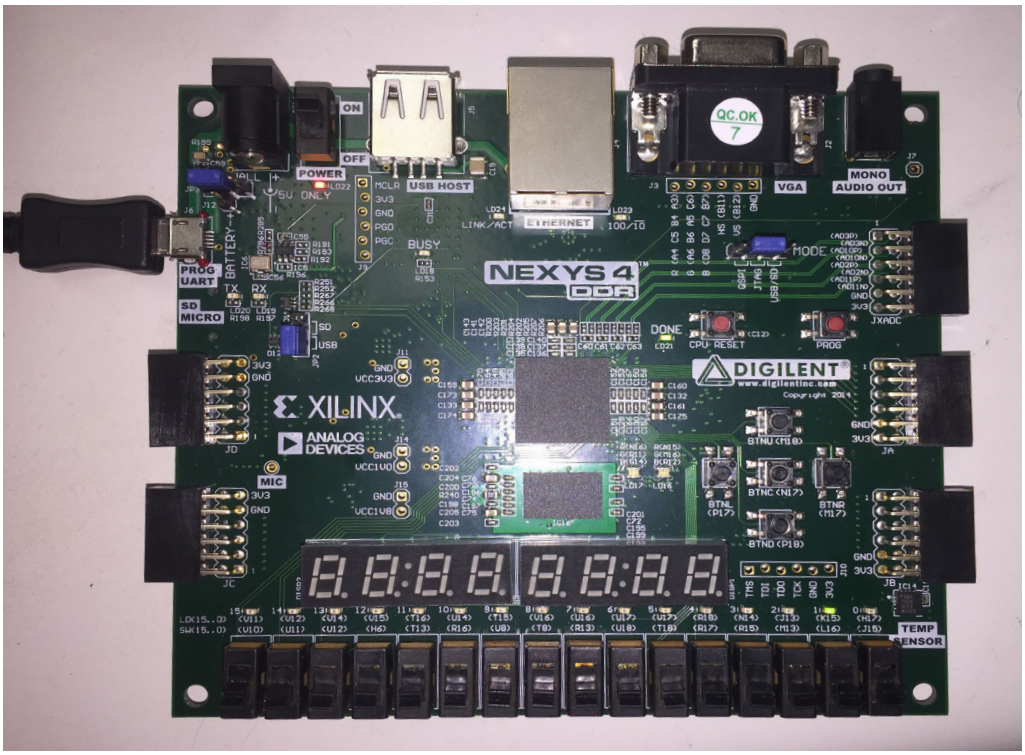

FIG. 1. Diligent NEXYS4-DDR Artix-7 test board.